



07-28-05

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT		Docket Number: 10746/23	
Application Number 09/754,632	Filing Date January 4, 2001	Examiner David Lam	Art Unit 2827
Title FUNCTION RECONFIGURABLE SEMICONDUCTOR DEVICE AND INTEGRATED CIRCUIT CONFIGURING THE SEMICONDUCTOR DEVICE		Applicant(s) Kazuo AOYAMA et al.	

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicants hereby officially cite the following references listed on the PTO-1449 which were previously disclosed in the above-identified patent application.

To the extent applicable, this Supplemental Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(i), which provides that an Information Disclosure Statement that does not otherwise comply with 37 C.F.R. § 1.97 and § 1.98 will be placed in the file. The references are previously disclosed in the above-identified application to the Office.

2. While no fee is believed to be due for this Supplemental IDS, to the extent that the references are further considered, the Commissioner is hereby authorized to charge payment of any appropriate fees that may be required to the deposit account of **Kenyon & Kenyon**, deposit account number **11-0600**. A duplicate of this sheet is enclosed.

3. A copy of each patent, publication or other information listed on the modified PTO form 1449 is being provided.

Dated:

7/26/2005

By:

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EV 320 19564445



SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO-1449		Docket Number 10746/23	
Application Number 09/754,632	Filing Date January 4, 2001	Examiner David Lam	Art Unit 2827
Title FUNCTION RECONFIGURABLE SEMICONDUCTOR DEVICE AND INTEGRATED CIRCUIT CONFIGURING THE SEMICONDUCTOR DEVICE		Applicant(s) Kazuo AOYAMA et al.	

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE*

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCL ASS	TRANSLATION
	3-6679	January 14, 1991	Japan			English abstract*

* Disclosed and discussed in specification

OTHER DOCUMENTS

EXAMINER INITIAL	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	DeHon, "DPGA-Coupled Microprocessors: Commodity ICs for the Early 21st Century", Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines, April 10-13, pp. 31-39 (1994)*
	Fujii, "A Dynamically Reconfigurable Logic Engine with a Multi-Context/Multi-Mode Unified-Cell Architecture", ISSCC, February, p. 364 (1999)*
	Kaviani and Brown, "The Hybrid Field Programmable Architecture", IEEE Design & Test of Computers, April-June, pp. 74-83 (1999)*
	McCulloch and Pitts, "A Logical Calculus of the Ideas Immanent in Nervous Activity", Bulletin of Mathematical Biology, Vol. 52, No.1/2, pp. 99-115 (1990)*
	Sueyoshi, "Present Status and Problems of the Reconfigurable Computing Systems - Toward the Computer Evolution", Technical Report of IEICE, VLD96-79, CPSY96-91, (1996-12)*

* Disclosed and discussed in specification

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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